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# APPLICATION FOR UNITED STATES LETTERS PATENT

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**FOR:** STRUCTURE AND METHOD FOR ULTRA-SMALL GRAIN SIZE POLYSILICON

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# STRUCTURE AND METHOD FOR ULTRA-SMALL GRAIN SIZE POLYSILICON

## BACKGROUND OF THE INVENTION

### *Field of the Invention*

The present invention generally relates to a semiconductor device and method therefor, and more particularly to a structure and method of ultra-small (e.g., within a range of about 10 nm to about 20 nm) grain size polysilicon.

### *Description of the Related Art*

State-of-the-art complementary metal oxide semiconductor (CMOS) gates are beginning to target 30nm lengths. Typical polysilicon grain sizes are in the 50nm range (e.g., see S. Wolf, Silicon Processing for the VLSI Era, Vol. 2, Lattice Press, 1990; U.S. Patent No. 6,294,442).

However, this 50nm grain size creates many problems including that the polysilicon is more bamboo-like along the gate lines, and conductivity/resistivity becomes more sensitive to grain size at this nano-scale level (e.g., conductivity/resistivity tracks with grain size).

More specifically, assume that one has a 30 nm grain size and a 30 nm gate polysilicon is etched so that across the width there is one grain (e.g., there is a single crystal along the width). The length of the gate may be microns long. Hence, there is a single crystal all along the gate in a cross-section. Thus, a ladder structure (e.g., a “bamboo-like” structure) is formed in which the width is very small, but the length may be very long. This is problematic because the resistance would be very large otherwise.

Another problem is that the diffusion of dopants in these "large-grain" polysilicon gates will probably be mostly through lattice diffusion (similar to that of crystalline silicon) which is relatively slow (e.g., typically about a factor of 10 slower than diffusion for polysilicon) and sufficient dopant may not reach the polysilicon/oxide interface, where dopant is also needed to prevent polysilicon depletion effects.

Further, one may have to increase thermal budgets enormously (e.g., to 1050 °C for about 5 seconds or the like, depending upon the dopants used, etc.) to cause dopants to reach the polysilicon/oxide interface and recoup this depletion loss, which then impacts channel doping adversely.

Therefore, for small gate lengths, it is very useful to have polysilicon with a much smaller average grain size of 10-20nm. However, prior to the present invention, such has not been achieved.

That is, it is well known that polycrystalline grain size may somewhat correlate with film thickness, and given that the typical gate stack thicknesses are in the 100nm range, it is difficult to limit the grain size to the 10-20nm range.

Indeed, all previous methods at controlling the average grain size through various deposition conditions have consistently yielded best defect-free material only in the ~50nm average grain size range.

Thus, prior to the present invention, there has been no method for making small nano-scale grained polysilicon with a concomitant structure that goes along with it.

## SUMMARY OF THE INVENTION

In view of the foregoing and other exemplary problems, drawbacks, and disadvantages of the conventional methods and structures, an exemplary feature of the present invention is to provide a method for making small nano-scale grained polysilicon with a concomitant structure that results therefrom.

In a first exemplary aspect of the present invention, a method of forming a semiconductor structure (and the resulting structure), includes providing a nitride layer between a silicon-containing layer and a polysilicon layer.

In a second exemplary aspect of the present invention, a method of making a semiconductor structure (and the resulting structure), includes forming a gate stack including a silicon-containing layer and a polysilicon layer with a nitride layer formed therebetween. The silicon-containing layer sets the polysilicon grain size.

In a third exemplary aspect of the present invention, a semiconductor structure, includes a first polysilicon layer, a second polysilicon layer formed over the polysilicon layer, and a nitride layer formed between the first and second polysilicon layers. A grain size of the first polysilicon layer is smaller than that of the second polysilicon layer.

With the unique and unobvious aspects of the present invention, ultra-small polysilicon grains at nano-scale size (e.g., within a range of about 10 nm to about 20nm) can be created, and their size can be retained through heat cycles.

Preferably, the invention deposits thin (e.g., 10-20nm) amorphous Si, or thin polysilicon or SiGe, with amorphous silicon being most preferable since it is harder to obtain precise polysilicon thickness control in the 10-20nm range, but very easy to obtain thin a-Si thickness control in this thickness range.

The invention also preferably deposits an ultra-thin (e.g., within a range of about 5-15Å) nitride barrier, which is known to be electrically conductive, is not a dopant diffusion barrier, and prevents polysilicon grain growth templating from single crystal silicon in straps in DRAMs.

Thereafter, preferably the invention grows the remaining polysilicon on the nitride barrier to set the correct gate stack thickness.

The present inventors have recognized that breaking the polysilicon film into two parts (e.g., first and second layers) where the first polysilicon layer sets the polysilicon grain size, is very advantageous in achieving such ultra small polysilicon grain size.

There are many advantages of the present invention including that it is very simple and inexpensive to integrate the present invention into the process. Additionally, the invention is applicable to any substrate, bulk or silicon-on-insulator (SOI), SiGe, etc.

Additionally, the inventive approach is readily detectable (and has been validated by the present inventors) because SIMS will show a nitrogen peak within the polysilicon and TEMs/SEMs will reveal small grains and an ultra-thin layer within the polysilicon.

Further, the small grain size facilitates dopant diffusion and reduces polysilicon depletion.

## BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other exemplary purposes, aspects and advantages will be better understood from the following detailed description of exemplary embodiments of the invention with reference to the drawings, in which:

Figures 1-3 illustrate processing steps of a first exemplary embodiment of the inventive method and specifically:

Figure 1 illustrates forming a gate dielectric and depositing a thin amorphous Si (~10-20nm);

Figure 2 illustrates depositing an ultra-thin (e.g., 5-15Å) nitride barrier at 550-750°C; and

Figure 3 illustrates depositing remaining needed polysilicon;

Figure 4 illustrates a second embodiment of the inventive method according to the present invention; and

Figure 5 illustrates a flowchart of the method 500 according to the present invention.

## DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS OF THE INVENTION

Referring now to the drawings, and more particularly to Figures 1-5, there are shown exemplary embodiments of the method and structures according to the present invention.

## EXEMPLARY EMBODIMENT

Again, as mentioned above, there are no known solutions to creating ultra-small polysilicon grains at nano-scale size (e.g., within a range of about 10nm to about 20nm), let alone retaining their size through heat cycles.

The present solution incorporates the idea of breaking the polysilicon film into two parts where the first layer sets the polysilicon grain size.

First, either thin (10-20nm) amorphous Si or thin polysilicon is deposited on a gate dielectric, which is typically formed on a substrate. Then, an ultra-thin (e.g., 5-15Å) nitride barrier is deposited on the a-Si or thin polysilicon. Such a nitride barrier is known to be electrically conductive, is not a dopant diffusion barrier, and has been known to prevent polysilicon

grain growth templating from single crystal silicon in straps in dynamic random access memories (DRAMs) or the like.

Then, the remaining polysilicon is grown (deposited) on the nitride barrier to set the correct gate stack thickness.

With the above in mind and turning now to the processing steps in greater detail, in a first embodiment, Figure 1 illustrates forming a gate dielectric 110 on a substrate 100. Preferably, the gate dielectric 110 has a thickness in a range within about 9 Å to about 50 Å. Preferably, the gate dielectric may be formed by any suitable dielectric such as an oxide, an oxynitride, an oxide-nitride stack combination, etc., and the like.

Thereafter, a thin silicon layer 120 (e.g., either a polysilicon or an amorphous Si, having a thickness on the order of about ~10-20nm) is deposited on the gate dielectric at a temperature typically below 550 °C.

Amorphous silicon is preferable since it is more difficult to get precise polysilicon thickness control in the approximate 10-20nm range, but very easy to get thin a-Si thickness control in the approximate 10-20 nm thickness range.

Then, as shown in Figure 2, an ultra-thin (e.g., on the order of about 5Å to about 15Å) nitride barrier 130 is formed (e.g., via, for example, a furnace anneal, in for example, an ammonia ambient (or typically referred to as an "$NH_3$ bake")) on the silicon layer 120 at a temperature within a range of about 550 °C to about 750 °C for about 5 minutes to about 20 minutes, and more preferably for about 15 minutes.

It is noted that methods other than the furnace anneal could be employed as would be known by one of ordinary skill in the art taking the

present application as a whole. The nitride barrier 130 is preferably silicon nitride.

It is noted that the 550-750°C temperature range is preferably used since the nitride layer is very thin, and a higher temperature (e.g., above 750 °C) would result in a thicker nitride. Thus, the above temperature range is believed to be the best. Additionally, a higher temperature would result in the amorphous silicon below (which begins to convert to polysilicon at about 550°C) to convert to polysilicon and would begin growing thicker and thicker. Hence, this approximate 550-750°C temperature range is used for obtaining the approximate 5-15 Å layer.

Thus, it is noted that a-Si will convert to polysilicon with about 10-20nm grain size. Reference numeral 125 illustrates the small grain (about 10-20 nm grain size) polysilicon layer in Figure 2.

Then, in Figure 3, remaining needed polysilicon 140 is deposited. The grain size here (e.g., of polysilicon 140) can be different (e.g., typically within a range of about 30 nm to about 80 nm), but the polysilicon layer 125 retains its grain size because of the ultra-thin nitride barrier.

It is noted that there is no limit to the thickness of the polysilicon 140 which is deposited, but typically it is within a range of about 80nm to about 130 nm. It is noted that the typical gate stack has a height (thickness) of about 100-150 nm. Additionally, while the choice of nitride as an insulator may appear unusual in certain contexts, it is noted that the nitride barrier layer does not pose an electrical or diffusion barrier in different applications (e.g., DRAM, etc.).

Thereafter, subsequent processes for gate and device building are performed, to complete the gate stack and device. That is, the polysilicon etch is performed including full gate stack etch, form extensions, form sidewall spacers, form source and drain, etc. Such processes are standard and conventional, and, for brevity, will not be further described herein.

Thus, this embodiment provides much smaller grain size which provides the higher activation. Additionally, the inventive process does not result in any substantial increase in thermal budget from process of building the conventional structures. There may be a slight increase in thermal budget due to the splitting of the gate into two parts (e.g., any additional thermal budget is due to the nitride layer), but this is unnoticeable since it is performed early in the gate building process (early in the gate stack).

**Second Embodiment**

Turning to Figure 4, a second embodiment of the inventive method is shown.

Specifically, Figure 4 illustrates a gate stack formed by the second embodiment in which the small grained polysilicon 125 of the first embodiment is replaced by a small-grained SiGe layer 425. In addition to the advantages of the first embodiment, this SiGe layer provides the additional advantage of better activation of the dopants (e.g., see Ozturk et al., International Workshop on Junction Technology, 2001, page 77).

More specifically, alternatively to the amorphous Si or the polysilicon for the first layer 125 in the first embodiment, the second embodiment of the

present invention recognizes that it is also advantageous if SiGe is used for the thin layer 125. That is, SiGe is known to have better dopant activation than the small grained polysilicon, and the activation could be even higher for ultra-small (e.g., approximately 10-20nm) grain poly-SiGe.

Hence, as shown in Figure 4, the process flow is the same as described above for the first embodiment, except that a poly-SiGe 425 is deposited on the gate dielectric first followed by the ultra-thin nitride barrier and the remaining needed polysilicon.

**THE GENERAL METHOD OF THE INVENTION**

Figure 5 shows a method 500 according to the present invention for practicing the first and second embodiments.

Specifically, a method 500 of forming a semiconductor structure, includes a step 510 of providing a silicon-containing layer (e.g., a layer containing any of an amorphous silicon, a polysilicon, and a SiGe layer, preferably having a small grain size) preferably on a gate dielectric. Thus, for purposes of the present application, "silicon-containing" includes any of an amorphous silicon, a polysilicon, and a SiGe layer.

If amorphous silicon or polysilicon is used as the silicon-containing layer (e.g., as in the first embodiment), then such amorphous silicon or polysilicon layer is preferably deposited at a temperature typically below 550°C. If the SiGe is deposited as the silicon-containing layer (e.g., the SiGe layer of the second embodiment), there is no such temperature constraint as in the first embodiment.

In step 520, a nitride layer is formed over the silicon-containing layer, preferably at a temperature between about 550°C and 750°C.

In step 530, a polysilicon layer (having any grain size desired) is formed over the nitride layer. Thus, the gate stack is formed. As mentioned above, to complete the device, the conventional device forming processes can be performed thereafter.

There are many advantages of the present invention including that it is very simple and cheap to integrate this into the process. Additionally, the invention is applicable to any substrate, bulk or SOI, or SiGe, strained silicon, etc.

Additionally, the inventive approach is readily detectable (and thus validated) because scanning ion mass spectroscopy (SIMS) will show a nitrogen peak within the polysilicon and TEMs/SEMs will reveal small grains and an ultra-thin layer within the polysilicon.

While the invention has been described in terms of several exemplary embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.

For example, in addition to the conductive materials described above, other conductive materials (e.g., such as possibly some refractory nitrides) could be substituted and the invention would still be highly advantageous.

Further, it is noted that, Applicant's intent is to encompass equivalents of all claim elements, even if amended later during prosecution.